AMENDMENTS

In The Specification

Please amend paragraph [0018] (the paragraph number is based on the E-filing version) as follows:

[0018] FIG. 2A schematically shows a power layer cut ichnography in the area where the north bridge control chip is coupled to the CPU in the preferred embodiment of the present invention; FIG. 2B is a cross-section view of FIG. 2A; and

Please amend paragraph [0020] as follows:

[0020] In order to support both 423 and 478 pin Intel Pentium IV CPUs, the layout structure of the preferred embodiment according to the present invention configures the area where the control chip is coupled to the CPU on the 4 layers motherboard from up to down sequentially as a top signal layer, a grounded layer having a grounded potential, a power layer, and a bottom solder layer. Wherein, the power layer comprises a first reference area having a grounded potential and a second reference area having different interface operating voltage sources. FIG. 2A and FIG. 2B schematically shows a power layer cut ichnography in the preferred embodiment of the present invention. From FIG. 2A and FIG. 2B, the power layer where the north bridge control chip 202 is coupled to the CPU 200 has been cut off to constitute a first reference area 204 and a second reference area 206. The first reference area 204 is placed near the right hand side 208 of the north bridge control chip 202 (i.e. the side nearest the CPU 200), it is also the area coupled to the grounded potential; the second reference area 206 is placed in the area that is formed from the north bridge control chip 202 cutting into the upper side 210 (the upper side 210 and the right hand side 208 are contiguous sides), it is also the area coupled to the CPU operating voltage (all other interface operating voltages are not shown in the diagram).